REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Non-Final Office Action of May 20, 2003 has been received and its contents carefully reviewed.

In the Non-Final Office Action of May 20, 2003, the Examiner rejected claims 1-5, 8-11, and 15-17 under 35 U.S.C. §102(b) as being anticipated by Matsuo et al. (U.S. Pat. No. 4,319,237); rejected claims 12 and 14 under 35 U.S.C. §103(a) as being unpatentable over Matsuo et al. in view of Berting et al. (U.S. Pat. No. 4,393,379); and objected to claims 6 and 13 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The rejections of these claims are traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

Applicants appreciate the indication of allowable subject matter in claims 6 and 13, which were objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

The rejection of claims 1-5, 8-11, and 15-17 under 35 U.S.C. §102(b) as being anticipated by Matsuo et al. is respectfully traversed and reconsideration is respectfully requested.

Preliminarily, Applicants note that claims 1-11 and 15-17 were rejected by the Examiner under "35 U.S.C. § 102(b) as being anticipated by [Matsuo et al.] (U.S. Pat. No. 6,236,385)." Applicants respectfully submit, however, that the Matsuo et al. is designated by U.S. Pat. No. 4,319,237 while Nomura et al. is designated by U.S. Pat. No. 6,236,385. For

purposes of prosecution, and in view of the actual rejection of the aforementioned claims, Applicants hereby assume the Examiner intended to reject claims 1-5, 8-11, and 15-17 under 35 U.S.C. § 102(b) as being anticipated by Matsuo et al.

Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "...resetting each liquid crystal cell of the liquid crystal display device simultaneously." None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that independent claim 1 and claims 2 and 3, which depend therefrom are also allowable over the cited references.

In rejecting claim 1, the Examiner cites Matsuo et al. as teaching "...resetting each liquid crystal cell of the liquid crystal display device simultaneously (note in figure 12, and column 8, lines 21-27, Matsuo teaches about the erasing signal applied to the common electrode terminal 8). The erasing signal resets each LCD cell simultaneously."

Further, in the "Response to Arguments" section of the Office Action dated May 20, 2003, the Examiner states "Matsuo ...teaches about... resetting each liquid crystal cell of the liquid crystal display device simultaneously (note in figure 12, and column 8, lines 21-27, Matsuo teaches about the erasing signal applied to the common electrode terminal 8)."

Applicants respectfully submit, however, Matsuo et al. does not describe, either inherently or explicitly, at least the aforementioned combination of elements with respect to independent claim 1.

For example, Applicants respectfully submit that while Matsuo et al. states with reference to Figure 13 at column 8, lines 21-27, "[i]n the scattering state variation of (E), a continuous line the variation when the erasing AC signal is applied to the common electrode

terminal 8...," the erasing AC signal, however, does not reset "each LCD cell simultaneously," as asserted by the Examiner.

More specifically, Matsuo et al. states at column 4, lines 41-44 "...the AC generating circuit 33 applies an AC signal of about 15 KHz ...as an erasing signal to the liquid crystal cell 26," and at column 4, lines 49-50, "[t]he application of the AC signal of about 15 KHz considerably improves the decay time," where the "decay time" is defined at column 3, lines 65-67 in Matsuo et al. as "...a time taken for returning the scattering state to the original state when the DSM liquid crystal is used." The only passage where Matsuo et al. teaches resetting LCD cells occurs at column 4, lines 17-18, stating "[r]eference numeral 32 is a reset signal source to reset the capacitor 27" and at column 4, lines 36-40, stating "...using the period of 5 ms at the end of each frame, the reset signal source sequentially applies reset signals to the capacitors, through the electrode lines 29 and the diodes 23 thereby to reset the capacitors 27 to zero level."

Accordingly, Applicants respectfully submit the erasing AC signal of Matsuo et al. does not reset each LCD cell simultaneously, as asserted by the Examiner. Rather, the erasing AC signal of Matsuo et al. merely improves a time taken for returning the scattering state to the original state when a particular type of liquid crystal is used.

Accordingly, Applicants respectfully submit Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 1.

Claim 4 is allowable over the cited references in that claim 4 recites a combination of elements including, for example, "wherein a reset voltage is applied to all liquid crystal cells of the liquid crystal display device to reset the liquid crystal display device". None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least

this feature of the claimed invention. Accordingly, Applicants respectfully submit that independent claim 4 and claims 5-8, which depend therefrom are also allowable over the cited references.

In rejecting claim 4, the Examiner cites Matsuo et al. as teaching a method "wherein a reset voltage is applied to all liquid crystal cells of the liquid crystal display device to reset the liquid crystal display device (col. 8, lines 21-27)."

Applicants respectfully submit, however, Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 4. Similar arguments made above with respect to claim 1 are equally applicable with respect to the rejection of claim 4. Accordingly, Applicants respectfully submit Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 4.

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, "[a] reset circuit for a liquid crystal display device, comprising: voltage selecting means for selecting...a normal common voltage to be applied... in an interval when a data voltage is charged and maintained in all liquid crystal cells of the liquid crystal display, and for selecting... a reset voltage less than the normal common voltage to be applied to the common electrode in a reset interval." None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least these features of the claimed invention.

In rejecting claim 9, the Examiner stated "[claim 9] ...has substantially the same limitations of claims 1-3, therefore, it is analyzed as previously discussed in claims 1-3 above."

Applicants respectfully submit, however, Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 9. Similar arguments made above with respect to claims 1 and 4 are equally applicable with respect to the rejection of claim 4. Accordingly, Applicants respectfully submit Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 9.

Claim 10 is allowable over the cited references in that claim 10 recites a combination of elements including, for example, "a voltage amplifier for amplifying an input control signal having a specific logical state only in a reset interval when liquid crystal cells of the liquid crystal display device are reset..." None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that independent claim 10 and claim 11, which depends therefrom are also allowable over the cited references.

In rejecting claim 10, the Examiner cites Matsuo et al. as showing, with respect to Figures 12 and 15, "...a reset circuit... comprising... a voltage amplifier (note the voltage applied to input 54 is amplified by transistor 60) for applying an input control signal having a specific logical state only in a reset interval ...(col. 10, lines 3-10)."

Applicants respectfully submit, however, that Matsuo teaches at column 10, lines 3-10 "...the erasing AC signal applied to the input terminal is amplified by the transistor 60." Accordingly, Applicants respectfully submit that Matsuo et al. does not teach or suggest at least the aforementioned combination of elements. Further, similar arguments presented above with respect to the rejections of claims 1, 4, and 9 are equally applicable with respect to the rejection of claim 10.

Claim 15 is allowable over the cited references in that claim 15 recites a combination of elements including, for example, "means for simultaneously resetting all of the liquid crystal cells". None of the cited references, including Matsuo et al., singly or in combination, teaches or suggests at least this feature of the claimed invention. Similar arguments presented above with respect to claims 1 are also applicable with respect to claim 15. Accordingly, Applicants respectfully submit that independent claim 15 and claims 16 and 17, which depend therefrom are also allowable over the cited references.

In rejecting claim 15, the Examiner stated claim 15 "...has substantially the same limitations of claims 1-2, therefore, [it] is analyzed as previously discussed in claims 1-2 above."

Applicants respectfully submit, however, Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 15. Similar arguments made above with respect to claims 1, 4, 9, and 10 are equally applicable with respect to the rejection of claim 15. Accordingly, Applicants respectfully submit Matsuo et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 15.

The rejection of claims 12-14 under 35 U.S.C. § 103(a) as being unpatentable over Matsuo et al. in view of Berting et al. (U.S. Pat. No. 4,393,379) is respectfully traversed and reconsideration is respectfully requested.

Claim 12 is allowable over the cited references in that claim 12 recites a combination of elements including, for example, "logical OR gates for performing a logical OR operation of an input reset signal and each gate driving signal from the shift register." None of the cited references, including Matsuo et al. or Berting et al., singly or in combination, teaches or

suggests at least this features of the claimed invention. Accordingly, Applicants respectfully submit that independent claim 12 and claims 13 and 14, which depend therefrom are also allowable over the cited references.

The Examiner cites Matsuo et al. as teaching "a reset circuit for a liquid crystal display device (col. 8, lines 21-27)" and admits "[Matsuo et al.] fails to teach about a shift register, logical OR gates for performing a logical OR operation of an input reset signal and each gate driving signal from the shift register..." The Examiner then cites Berting et al. as teaching the limitations that were not disclosed by Matsuo et al., citing to Figures 1 and 2 and column 2, line 55 – column 3, line 4 of Berting et al. Lastly, the Examiner concludes that "it would have been obvious to... improve upon the non-multiplexed LCD drive circuit, as disclosed by [Berting et al.]. Doing so would provide a low cost LCD drive circuit that is suitable for instrumentation applications."

Applicants respectfully submit, however, that Berting et al. teaches at column 2, line 55 – column 3, line 4 "Shift register 14 is of conventional type having a number of parallel output terminals 11 corresponding to the number of LCD electrical lines to be driven. The shift register 14 could, for example, comprise a number of tandomly connected four bit static shift registers... parallel output lines 11_1-11_n, a serial input terminal 13a and a serial output terminal 13b. ...The contents of the shift register 14 are reset or cleared by application of a logic zero signal to CLEAR terminal 19."

Accordingly, Applicants respectfully submit that neither Matsuo et al. nor Berting et al., either singly or in common, teach or suggest at least the aforementioned combination of elements. Further, Applicants respectfully submit Berting et al. is directed to "non-multiplexed LCD driver circuitry have data update and refresh capabilities." (see Berting et

al., column 1, lines 6-7) Accordingly, Applicants respectfully submit the Examiner's aforementioned conclusion "it would have been obvious to... improve upon the non-multiplexed LCD drive circuit, as disclosed by [Berting et al.]. Doing so would provide a low cost LCD drive circuit that is suitable for instrumentation applications" does not provide any motivation to modify Matsuo et al. with Berting et al.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

Respectfully submitted,

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